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WO 87/00688 A1 US 4914056 A
Abstract of JP63076350, Patent Abstracts of Japan, Vol.12, No.308, page 127 & JP63076350

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(71) Applicant(s)
Mitsubishi Denki Kabushiki Kaisha
(Incorporated in Japan)
No. 2-3 Marunouchi 2-chome, Chiyoda-ku,
Tokyo 100-8310, Japan

Ryoden Semiconductor System Engineering Corporation
(Incorporated in Japan)
1 Mizuhara 4-chome, Itami-shi, Hyogo 664, Japan

(72) Inventor(s)
Hiroyuki Shima

(74) Agent and/or Address for Service
Beresford & Co
2-5 Warwick Court, High Holborn, LONDON,
WC1R 5DJ, United Kingdom

(54) Abstract Title

Semiconductor device having wiring layers integrally formed with an interlayer connection plug, and method of manufacturing the same

(57) To form an interconnection between an upper wiring layer 9 and a lower wiring layer 8 of a semiconductor device, a conductive material 7, 8, which may comprise more than one layer, but has uniform etching characteristics is deposited in a trench formed in an insulation film 3 that will insulate the upper wiring layer from the lower wiring layer. The lower wiring layer and the plug are etched form the deposited conductive material using a resist pattern. The wiring structure does not include an etching stopper at the boundary between the lower wiring layer and the plug.

FIG. 1B

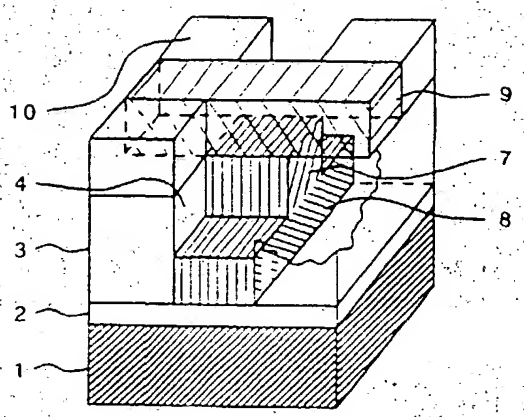

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FIG . 1A

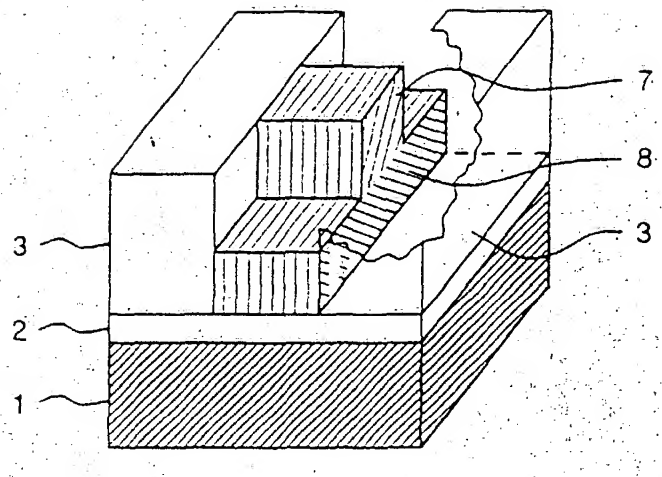


FIG . 1B

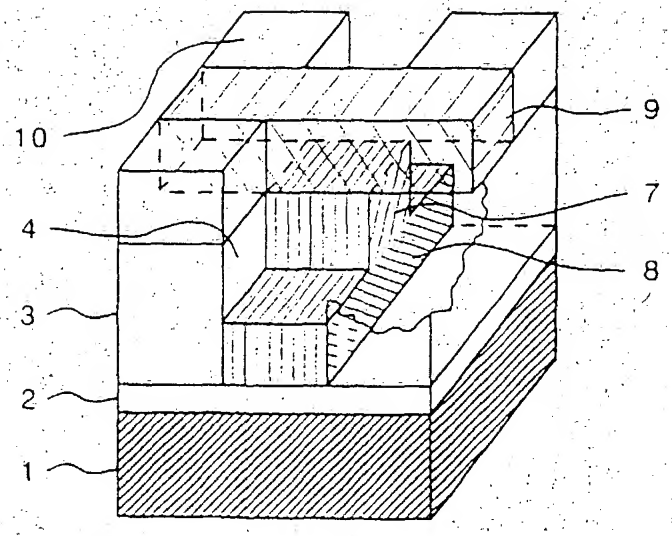


FIG. 2A

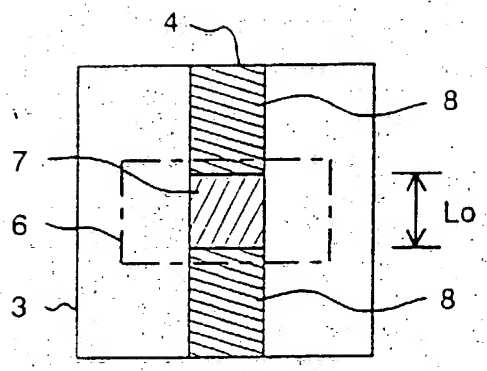


FIG. 2B

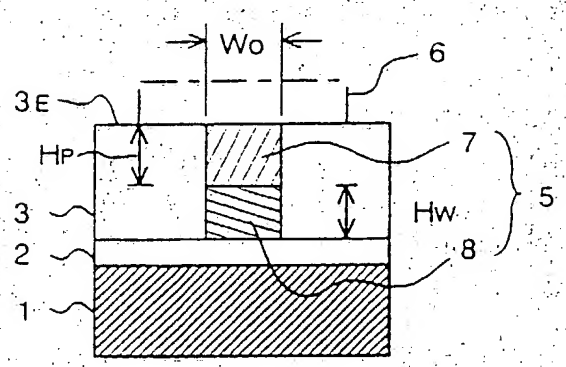


FIG. 2C

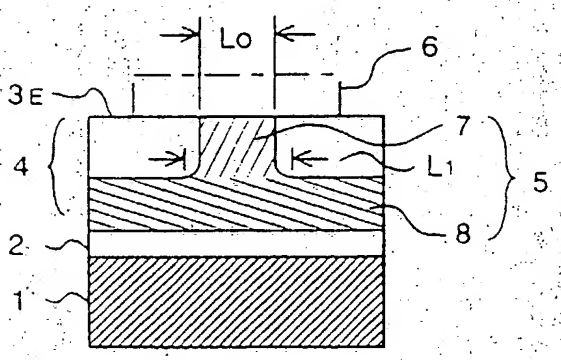


FIG. 3A

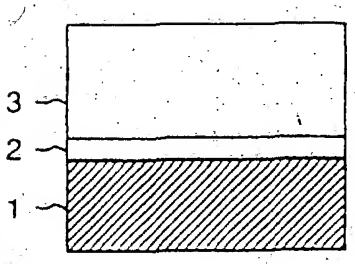


FIG. 3B

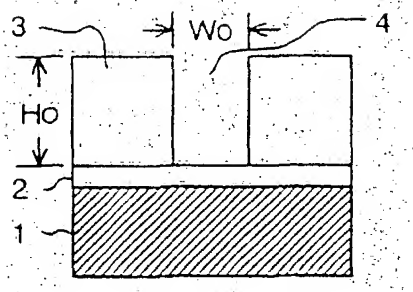


FIG. 3C

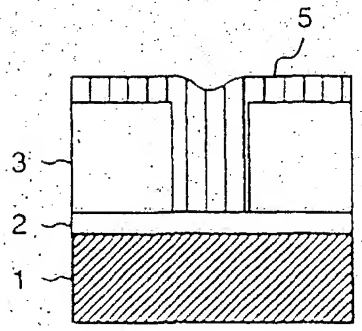


FIG. 3D

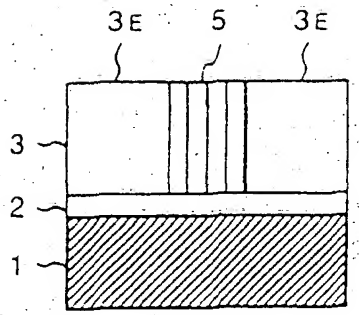


FIG. 3E

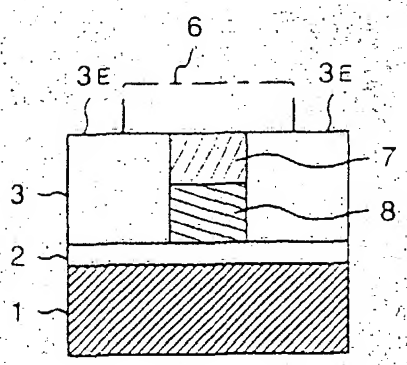


FIG. 3F

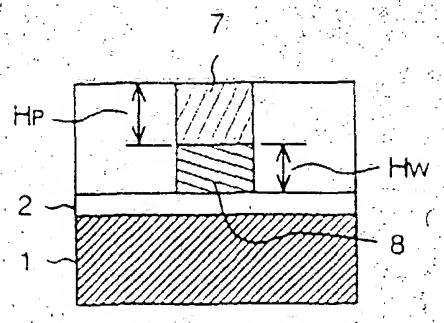


FIG . 4

(PRIOR ART)

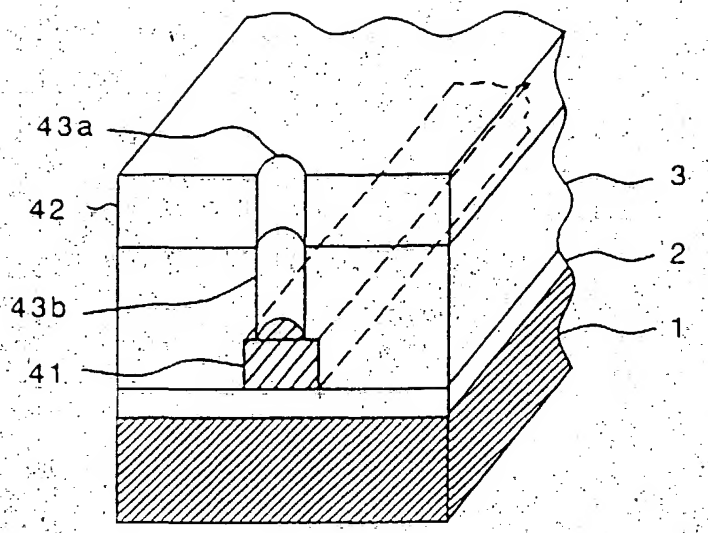


FIG. 5A

(PRIOR ART)

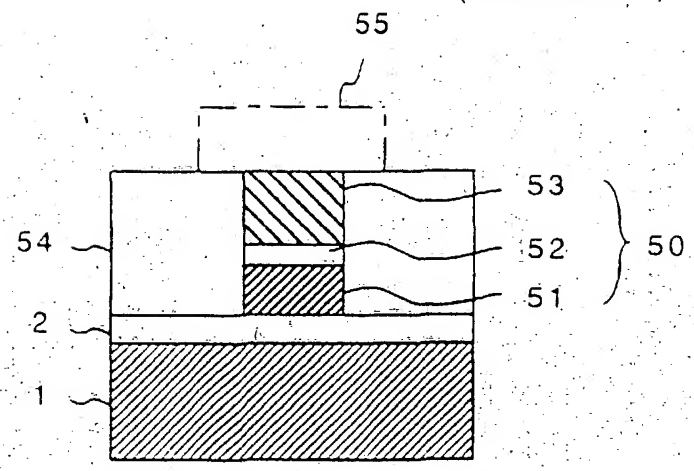
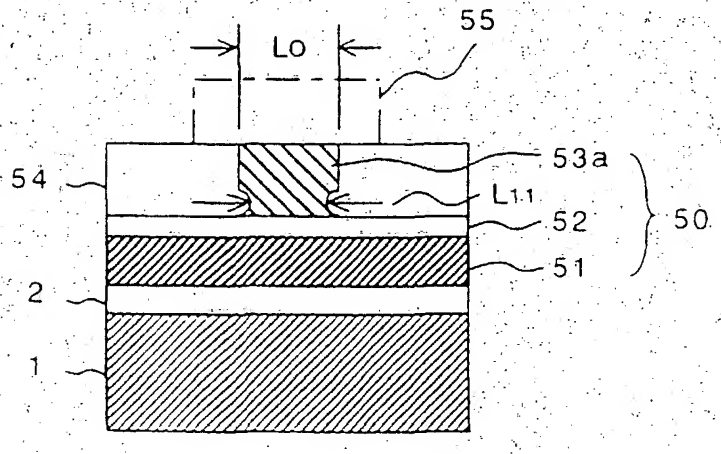


FIG. 5B

(PRIOR ART)



SEMICONDUCTOR DEVICE HAVING WIRING LAYERS INTEGRALLY FORMED WITH AN INTERLAYER CONNECTION PLUG AND METHOD OF MANUFACTURING THE SAME

Technical Field

The present invention relates to a semiconductor device and a method of manufacturing the same. More particularly, the present invention relates to a semiconductor device having a multilayer wiring structure which includes an upper wiring layer, a lower wiring layer, and a columnar connection section (hereinafter referred to as a plug) for connecting them, as well as to a method of manufacturing the semiconductor device.

Background Art

A method of forming a plug, which is also called a columnar connection section (i.e., a columnar protuberance) or a through-hole plug and used for connecting a lower wiring layer to an upper wiring layer within a multilayer wiring structure, is disclosed, for example, in Japanese Patent Application Laid-open Nos. 63-76350, 5-47935, or 9-69559.

FIG. 4 shows one example of the structure of an interlayer connection within a conventional semiconductor device. As shown in FIG. 4, a first interlayer insulation film 2 is formed on a semiconductor substrate 1, and a lower wiring layer 41 is formed on the first interlayer insulation film 2. A second interlayer insulation film 3 is stacked on the first interlayer insulation film 2 so as to enwrap the lower wiring layer 41. In order to form a vertical connection section for

establishing a connection between the lower wiring layer 41 and an upper wiring layer (not shown) formed on the second interlayer insulation film 3, a resist mask 42 is formed on the second interlayer insulation film 3. An opening 43a used for the purpose of forming a through hole is formed in the resist mask 42. The second interlayer insulation film 3 is etched through the opening 43a, to thereby form a through hole 43b leading up to the lower wiring layer 41.

The resist mask 42 is then removed, and electrical contact is established between the lower wiring layer 41 and the upper wiring layer by filling the through hole 42 with electrically-conductive material.

Under such a conventional method of forming a multilayer wiring structure, as the diameter of the through hole becomes smaller, an opening failure is apt to arise during the patterning of a resist mask used for the purpose of opening a through hole. Further, due to a decrease in the size of the lower-layer wiring patterns and the pitch between the patterns, a positional displacement of an opening of a through hole is apt to arise.

FIGs. 5A and 5B are cross sectional views for explaining another multilayer wiring structure of another conventional semiconductor device. FIG. 5A is a front cross-sectional view of the semiconductor device, and FIG. 5B is a side cross-sectional view of the same. As shown in FIG. 5A, the first interlayer insulation film 2 is formed on the semiconductor substrate 1. Next, a plurality of conductive members 50 are formed on the first interlayer insulation film 2 at given intervals and in parallel with each other. Each of the conductive members 50 comprises a lower wiring layer 51, an etching stopper 52, and a plug member 53 to be used as a plug, all of which are stacked in this order. Subsequently, a

second interlayer insulation film 54 is filled into the clearance between the conductive members 50.

A resist pattern 55, which is slightly larger than a through-hole plug to be formed, is formed on each conductive member 50. While the resist pattern 55 is used as an etching mask, the plug member 53 is etched to thereby form the lower wiring layer 51 and the through-hole plug 53a, as represented by a side cross-sectional view of FIG. 5B.

In the manufacture of a semiconductor device having such a structure, the etching stopper 52 stops the etching of the plug member 53. However, since the plug member 53 is etched in an isotropic manner, there arises a risk of the width Lo of the through-hole plug 53a being reduced to a smaller width L11 as a result of over-etching of the area of the through-hole plug 53 in the vicinity of the etching stopper 52.

Further, the manufacture of a semiconductor device having such a conventional multilayer wiring structure involves the need to form the etching stopper 52 between the lower wiring layer 51 and the plug member 53, thereby complicating the formation of the conductive member 50. Further, switching between isotropic etching and anisotropic etching makes the etching process complicated.

Disclosure of the Invention

The present invention has been contrived to solve the foregoing drawbacks in the background art, and the primary object of the present invention is to provide a semiconductor device which has superior characteristics and is formed from a conductive member having a lower wiring layer integrally formed with an interlayer connection plug.

The second object of the present invention is to provide a method of manufacturing a semiconductor de-ice

having a simplified step of forming a plug used for the purpose of connecting multilayer wiring patterns together.

To accomplish these objects, in accordance with one aspect of the present invention, there is provided a semiconductor device comprising an upper wiring layer and a lower wiring layer which are spaced apart at a given interval within an interlayer insulation film; a columnar connection section which is formed substantially perpendicularly to the upper and lower wiring layers so as to connect the upper and lower wiring layers together; and the lower wiring layer and the columnar connection section being defined by a single piece conductive member of single layer or multi-layer structure (i.e. they are simultaneously formed).

Preferably, in the semiconductor device according to the present invention, the primary material of the conductive member consists of one or more materials selected from the group comprising polycrystalline silicon, aluminium, copper, cobalt, titanium, molybdenum, and tungsten.

Since members which are to become a lower wiring layer and a plug are formed by single deposition of a conductive material or materials, a structure having a high degree of reliability can be obtained.

Preferably, in the semiconductor device according to the present invention, the lower wiring layer and the columnar connection section are formed of either the same material or a plurality of materials having substantially the same etching characteristics at least at the juncture of the lower wiring layer and the columnar connection section.

In this case, a boundary region between the lower wiring layer and the plug is formed from one material or a plurality of materials having substantially the same etching characteristics, and does not include a material that acts as an etching stopper due to which etching

characteristics will drastically change. Accordingly, there is prevented formation of a width-reduced portion at the juncture of the lower wiring layer and the plug, thereby resulting in a plug having a high degree of reliability.

Preferably, in the semiconductor device according to the present invention, the width of the columnar connection section in the longitudinal direction of the lower wiring layer gradually increases toward the lower wiring layer.

In this case, since connection through a wide area is ensured between the lower wiring layer and the plug, a high degree of electrical and mechanical reliability can be attained.

In accordance with another aspect of the present invention, there is provided a method of manufacturing a semiconductor device comprising the steps of forming a trench in an interlayer insulation film formed on a semiconductor substrate; filling the inside of the trench with a conductive member; forming on the surface of the conductive member a resist pattern to be used for masking columnar connection section; and etching the conductive member to a given depth while using the resist pattern as a mask, thereby forming, from the conductive member, a lower wiring layer and a columnar connection section.

In the method, since a member which is to become a lower wiring layer and a plug can be formed from conductive material by a single deposition, a process of manufacturing a multilayer wiring structure can be simplified or shortened, and a structure having a high degree of reliability is obtained.

Further, since a displacement is not apt to arise in the position where a wiring layer and a plug overlap each

other, rendering photolithography for plug forming purposes is made easy.

The method may comprise the steps of removing the resist pattern and forming an upper wiring layer on the columnar connection section.

In this case, a connection is established between a lower wiring layer and an upper wiring layer, thereby yielding a semiconductor device having a multilayer structure.

In the method, etching of the conductive member is preferably performed by anisotropic etching.

In this case, a plug can be formed solely by anisotropic etching, and hence there can be formed a wiring structure which has a high degree of dimensional accuracy and reduced errors.

Brief Description of Drawings

FIGs. 1A and 1B are perspective views showing the structure of a semiconductor device according to a first embodiment of the present invention, particularly the structure of a lower wiring layer and a plug;

FIG. 2A is a plan view showing the structure of the semiconductor device according to the first embodiment, particularly the structure of a lower wiring layer and a plug;

FIG. 2B is a front cross-sectional view showing the same;

FIG. 2C is a side cross-sectional view showing the same;

FIGs. 3A to 3F are front cross-sectional views showing the steps of a method of manufacturing the semiconductor device according to the first embodiment;

FIG. 4 is a schematic representation for explaining the structure of an interlayer connection of a conventional semiconductor device and a method of manufacturing the device; and

FIGs. 5A and 5B are cross sectional views for explaining the structure of interlayer connection of another conventional semiconductor device and the manufacture of the device.

Best Mode for Carrying out the Invention

With reference to the accompanying drawings, preferred embodiments of the present invention will be described. Throughout the drawings, like or corresponding elements are assigned like reference numerals.

First Embodiment:

FIGs. 1A and 1B and FIGs. 2A through 2C show the structure of a semiconductor device according to a first embodiment of the present invention. FIG. 1 is a perspective view of the semiconductor device. More specifically, FIG. 1A shows a lower wiring layer and a columnar connection section (or a plug), and FIG. 1B shows an upper wiring layer formed on the plug.

FIGs. 2A through 2C are a plan view and cross-sectional views of the semiconductor device shown in FIGs. 1A and 1B. More specifically, FIG. 2A is a plan view, FIG. 2B a front cross-sectional view, and FIG. 2C a side cross-sectional view.

In FIGs. 1A and 1B, a first interlayer insulation film 2 is formed on a semiconductor substrate 1, and a second interlayer insulation film 3 is formed on the interlayer insulation film 2. A trench 4 is formed in the interlayer insulation film 3, and a lower wiring layer 8 is formed on the interlayer insulation film 2 at the bottom of the trench 4. An upper wiring layer 9 is formed on the interlayer insulation film 3. A columnar connection section (or a plug) 7 protrudes vertically from the lower wiring layer 8 until it comes into contact with the upper wiring layer 9, thereby connecting the

upper and lower wiring layers 8, 9 together. A third interlayer insulation film 10 is formed on the interlayer insulation film 4, and the upper wiring layer 9 is formed within the third interlayer insulation film 10.

With the foregoing structure, the conductive materials which are to form the lower wiring layer 8 and the plug 7 are formed at one time. In short, the conductive materials are integrally formed in one step or in a continuous series of steps. Accordingly, the conductive material is free from connection resistance and has superior electrical characteristics.

As shown in FIG. 2A, the lower wiring layer 8 has a width Wo, and the plug 7 is a prism fitted in the width Wo. The plug 7 has a length Lo in the longitudinal direction of the lower wiring layer 8.

Further, as shown in FIG. 2B, the lower wiring layer 8 has a height Hw, and the plug 7 has a height Hp.

As represented by the side cross-sectional view shown in FIG. 2C, the width of the plug 7 in the longitudinal direction of the lower wiring layer 8 increases toward the lower wiring layer 8 in the vicinity of the joint portion between the plug 7 and the lower wiring layer 8. As shown in the drawing, the maximum width of the width-increasing portion of the plug 7 is L1. Such a continuous structure renders the conductive material mechanically strong without an increase in electrical resistance and, hence, is very desirable.

Second Embodiment

FIGs. 3A - 3F are drawings for explaining the manufacture of a semiconductor device according to a second embodiment of the present invention. The manufacturing steps of the method are shown in the drawings, taking as an example the semiconductor device having a structure such as that described in the first embodiment.

The manufacturing method will now be described with reference to FIGs. 3A - 3F. First, as shown in FIG. 3A, the first interlayer insulation film 2 is formed from, for example, silicon oxide (SiO2), on the semiconductor substrate 1 made of silicon or the like. The semiconductor substrate 1 may have circuit elements and an electronic circuit formed therein. Next, the second interlayer insulation film 3 is formed on the first interlayer insulation film 2. The thickness of the second interlayer insulation film 3 is, for example, 1300 nm.

As shown in FIG. 3B, through use of photolithography and a dry etching technique, the trench 4 having a width Wo is formed in the interlayer insulation film 3. The width Wo of the trench 4 is set to, for example, 300 nm, as the width required by the lower wiring layer. The depth of the trench 4 is set so as to become equal to the thickness of the interlayer insulation film 3, for example, 1300 nm.

As shown in FIG. 3C, a conductive member 5 formed from, for example, tungsten, is deposited on the first interlayer insulation film 2 and the interlayer insulation film 3 by chemical vapor deposition such that the conductive member 5 fills the trench 4 and covers the top surface of the interlayer insulation film 3.

As shown in FIG. 3D, the excessive portion of the conductive member 5 is etched back. For example, excessive tungsten is etched back by sulfur hexafluoride (SF_6) gas, thereby exposing a surface 3E of the interlayer insulation film 3.

As shown in FIGs. 3E and 2A to 2C, a resist pattern 6 is formed by photolithography in an area on the surface of the conductive member 5, where the plug 7 for connecting the lower wiring layer 8 to the upper wiring layer 9 is to be formed. The conductive member 5 is etched while the resist pattern 6 is used as a mask. For

example, tungsten is etched by a SF_6 gas. FIG. 3E shows the conductive member as it is being etched.

As shown in FIGs. 3F and 2A to 2C, etching is controlled such that when the length of the plug 7 becomes Hp and the thickness of the lower wiring layer 8, which is made of the conductive material remaining on the bottom of the trench 4, becomes Hw, etching of the conductive member 5 is stopped. In this case, it is desirable to etch the conductive member by anisotropic etching so as to prevent the formation of side edges. As a result, a plug having vertical side surfaces can be formed.

For example, as mentioned previously, the trench 4 preferably has a depth of 1300 nm. Further, the height of the lower wiring layer 8 preferably has a height Hw of, for example, 500 nm, and the plug 7 preferably has a height Hp of, for example, 800 nm.

The lower wiring layer 8 and the plug 7 are simultaneously formed from the same conductive material through the aforementioned steps. The lower wiring layer 8 and the plug 7 are then etched to have respective final shapes.

As shown in FIG. 1B, while the trench 4, from which the conductive material is removed through etching, is filled, a third interlayer insulation film 10 is formed on the interlayer insulation film 3. A trench is formed in the interlayer insulation film 10 in such a way as to pass over the plug 7. The upper wiring layer 9 is formed in the trench. The lower wiring layer 8 is eventually connected to the upper wiring layer 9 via the plug 7, thereby forming a semiconductor device.

A multilayer wiring structure having three or more layers may be formed through repetition of the cycle of the foregoing manufacturing steps.

The aforementioned manufacturing method can be summarized as follows:

1) A trench used for the purpose of forming a lower wiring layer (or the first wiring layer) is formed in the interlayer insulation film. The depth of the trench is the sum of the depth required by the lower wiring layer and the depth required by the interlayer insulation film situated between the lower wiring layer and the upper wiring layer (or the second wiring layer).

2) The trench is filled with conductive material, and a resist pattern, which is the same in size as the through hole, is formed on the conductive material at a position corresponding to the position of the through hole.

3) The conductive material filled in the trench is etched via a resist pattern to such an extent that the conductive material is left on the bottom of the trench in the thickness required by the lower wiring layer, whereby there is formed a columnar connection section (or a plug) for connecting the upper and lower wiring layers together.

4) The resist pattern is removed, and an interlayer insulation film is formed while there is filled the trench from which the conductive material has been removed. The interlayer insulation film is made flat, as required. The upper wiring layer is formed on the interlayer insulation film and is connected to the columnar connection section (or a plug). As a result, the upper and lower wiring layers are connected together, thereby forming a multilayer wiring structure.

According to the foregoing manufacturing method, the lower wiring layer 8 and the plug 7 are simultaneously formed from the same material, and hence the process of manufacturing a semiconductor device having a multilayer wiring structure can be simplified. The quantity of foreign article, which appears at the time of deposition of conductive material such as tungsten, is reduced, and

a wiring layer having a high degree of reliability can be formed.

In the manufacture of a conventional through-hole plug such as that described with reference to FIG. 4, a plug is formed through the formation of a through hole. The conventional method requires the formation of a minute hole. In contrast, under the method according to the present embodiment, a resist pattern used when a through-hole plug is not a hole but a pattern left on conductive material, so that a through-hole plug is left after etching. Therefore, photolithography becomes easier.

As can be seen from FIG. 2C, the boundary between the plug 7 and the lower wiring layer 8 has a continuous curved surface. Further, it is seen that the length L1 of the boundary region is larger than the length L0 of the plug 7 in the longitudinal direction of the trench 4. Such a continuous structure is very desirable from mechanical and electrical viewpoints. According to the aforementioned manufacturing method, a connection structure having such a configuration can be formed.

Third Embodiment:

A method of manufacturing a semiconductor device and a semiconductor device manufactured by the method according to a third embodiment will be described.

Although the first and second embodiments have been described with reference to a case where tungsten is used as conductive material which is to be used as a lower wiring layer and a plug, other materials may be used as the conductive material.

In one example, in a step corresponding to the step shown in FIG. 3C, titanium (Ti) is deposited to a thickness of 100 nm by sputtering, thereby forming a thin titanium film on the bottom or side surfaces of the trench 4. Subsequently, copper containing aluminum alloy

is deposited to a thickness of 1000 nm, thereby forming a multilayer structure comprising two layers.

In the case of aluminum, this material may be etched only by anisotropic etching through use of chlorine (Cl_2) gas or boron chloride (BCl_3) gas. As with tungsten, the boundary region between the plug and the lower wiring layer can be formed so as to have a desirable continuous structure.

Even in a case where a multilayer structure of three layers was formed in the foregoing order from titanium nitride (TiN) or Ti+TiN in place of titanium (Ti), a similar desirable result was obtained.

As mentioned previously, a portion of the conductive material which is to become a lower wiring layer and a portion of the conductive material which is to become a plug are deposited simultaneously. The expression "simultaneously" used herein signifies both the case of simultaneous deposition of a single material and the case of integral deposition of different types of materials in subsequent steps in the same process.

It is also acknowledged that, in addition to tungsten and aluminum, polycrystalline silicon, copper, cobalt, titanium, or molybdenum can be used as the primary material of the conductive member having uniform etching characteristics. Further, as in the second embodiment, it is acknowledged that a multilayer structure may be formed from a plurality of materials selected from the above-described conductive materials.

If a two-layer structure comprising, e.g., either aluminum and titanium or polycrystalline silicon and tungsten, exists in the boundary region between the plug 7 and the lower wiring layer 8, the etching characteristics of the boundary region change drastically. In such a case, as can be seen from the conventional example shown in FIG. 3B, there arises a risk that a width-reduced portion is formed as a result

of over-etching. It is desirable that conductive material(s) having substantially the same etching characteristics be used for the boundary region between the plug and the lower wiring layer. In other words, material, which does not contain a material that can be used as an etching stopper, is desirable as conductive material.

As mentioned previously, in the present embodiment, the foregoing conductive materials can be used for a member which is to become a lower wiring layer and a plug.

CLAIMS:

1. A semiconductor device comprising:

an upper wiring layer and a lower wiring layer which are spaced apart at a given interval within an interlayer insulation film; and

a columnar connection section which is formed substantially perpendicularly to said upper and lower wiring layers so as to connect said upper and lower wiring layers together, wherein

said lower wiring layer and said columnar connection section are defined by a single piece conductive member of single layer or of multilayer structure.

2. The semiconductor device according to claim 1, wherein the primary material of said conductive member consists of one or more materials selected from the group comprising polycrystalline silicon, aluminium, copper, cobalt, titanium, molybdenum, and tungsten.

3. The semiconductor device according to claim 1 or 2, wherein said lower wiring layer and said columnar connection section are formed of either the same material, or a plurality of materials having substantially the same etching characteristics at least at the juncture of said lower wiring layer and said columnar connection section.

4. The semiconductor device according to claim 1, 2 or 3, wherein the width of said columnar connection section in the longitudinal direction of said lower wiring layer gradually increases toward said lower wiring layer at the juncture of said lower wiring layer and said columnar connection section.

5. A semiconductor device as defined by claim 1 constructed substantially as described hereinbefore with reference to and as shown in Figures 1A to 2C or in Figures 1A, 1B, 3A to 3F.

6. A method of manufacturing a semiconductor device comprising the steps of:

forming a trench in an interlayer insulation film formed on a semiconductor substrate;

filling the inside of said trench with a conductive member;

forming on the surface of said conductive member a resist pattern to be used for masking a columnar connection section; and

etching said conductive member to a given depth while using said resist pattern as a mask, thereby forming, from said conductive member, a lower wiring layer and the columnar connection section.

7. The method of manufacturing a semiconductor device

according to claim 6, further comprising the steps of removing said resist pattern; and forming said upper wiring layer on said columnar connection section.

8. The method of manufacturing a semiconductor device according to claim 6 or 7, wherein said conductive member is etched by anisotropic etching.

Amendments to the claims have been filed as follows

1. A method of manufacturing a semiconductor device comprising the steps of:

forming a trench in an interlayer insulation film formed on a semiconductor substrate;

filling the inside of said trench with a unilayer conductive member of a single material;

forming on the surface of said conductive member a resist pattern to be used for masking a columnar connection section;

etching said conductive member to a given depth while using said resist pattern as a mask, thereby forming, from said conductive member, the columnar connection section, and a lower layer wiring;

removing said resist pattern; and

forming upper layer wiring on said columnar connection section.

2. A method of manufacturing a semiconductor device comprising the steps of:

forming a trench in an interlayer insulation film formed on a semiconductor substrate;

filling the inside of said trench with a multilayer conductive member of different materials to form a columnar connection section and a lower layer wiring;;

forming on the surface of said conductive member a resist pattern to be used for masking the columnar

connection section;

etching said conductive member to a given depth while using said resist pattern as a mask, using as etchant an etchant for which said different materials of said multilayer conductive member have substantially the same etching characteristics at least at the juncture of the columnar connection section and lower layer wiring to be formed, thereby forming, from said conductive member, the columnar connection section and the lower layer wiring;

removing said resist pattern; and

forming said upper wiring layer on said columnar connection section.

3. A semiconductor device comprising:

an upper layer wiring and a lower layer wiring which are spaced apart at a given interval within an interlayer insulation film; and

a columnar connection section which is formed substantially perpendicularly to said upper and lower layer wirings so as to connect said upper and lower layer wirings together, wherein

said lower layer wiring and said columnar connection section are formed from a common member of the same conductive material throughout.

4. A semiconductor device comprising:

section in the longitudinal direction of said lower layer wiring gradually increases toward said lower wiring layer at the juncture of said lower wiring layer and said columnar connection section.

8. A semiconductor device as defined by either of claims 3 or 4, constructed substantially as described hereinbefore with reference to and as shown in Figures 1A to 2C or in Figures 1A, 1B, 3A to 3F.